AD 292 317

RESEARCH REPORT
REPORT 1144
31 OCTOBER 1962

292 317

NEL/Report 1144

MICROELECTRONIC LOGIC IMPLEMENTATION FOR THE AN/UYK-1 COMPUTER

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THE PROBLEM

Investigate some of the technical, operational, and cost problems involved in the microminiaturization of portions of the AN/UYK-1 computer. In particular, investigate the feasibility of constructing the logic section of the computer with integrated circuit elements.

RESULTS

1. Construction of the AN/UYK-1 state counter with integrated circuitry showed that integrated elements operate satisfactorily at the AN/UYK-1 frequency of 0.33 Mc/s.

2. The integrated circuit elements tested tolerated power supply variations of at least ±30 per cent.

3. The operation of the integrated circuit elements was not affected by noise in the breadboard circuits.

4. The integrated circuit devices were relatively expensive, but prices have since been reduced and further reductions are expected. However, the economic feasibility of building the logic portions of the computer with integrated circuit devices depends not only on component cost but also on assembly costs, size of throw-away package, and other production costs which were not considered in this investigation.

RECOMMENDATIONS

1. Investigate memory accession requirements and the feasibility of using integrated circuit devices in memory accession circuits.

2. Conduct studies of the practicality of using integrated circuit elements in input/output buffer applications.

3. Perform further research to determine the extent of cross talk and noise problems involved in large-scale use of microelectronic devices.

ADMINISTRATIVE INFORMATION

Work was performed under BuWeps Task Assignment 48415 (NEL R2-2), partially funded by BUSHIPS Subproject SR 008 03 03, Task 9632, by members of the Data Control and Microsystems Division. This report covers the period September 1961 to June 1962 and was approved for publication 31 October 1962.

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ILLUSTRATIONS (Continued)

INTRODUCTION

This report describes the investigation of some of the technical, operational, and cost problems involved in microminiaturization of portions of the AN/UYK-1 computer by implementing certain of the AN/UYK-1 logic functions with integrated circuitry.

The forms of integrated circuits used in the study included the products of three manufacturers: Fairchild Semiconductor; Texas Instruments, Inc.; and General Instrument Semiconductor. Work involved familiarization with the operating characteristics of each of the integrated circuit devices and use of the devices in the functional reproduction of portions of the AN/UYK-1 logic circuits.

The AN/UYK-1 state counter was selected in each case because it consists of flip-flop and gate circuits, which are representative of logic circuits used throughout the computer and can be readily reproduced using off-the-shelf integrated circuit elements.

In addition, the AN/UYK-1 R-S flip-flop card was functionally duplicated using integrated circuit components. Although extensive implementation of the AN/UYK-1 logic is not feasible on a card-for-card basis, duplication of the R-S flip-flop card allowed performance of dynamic tests because the card could be inserted in the computer cabinet.

AN/UYK-1 STATE COUNTER SIMULATOR

In order not to involve, at least initially, the computer itself, standard AN/UYK-1 cards were obtained from Ramo-Wooldridge and a state counter simulator was built to provide logic driving signals for the integrated circuit elements

and to permit direct comparison of operating characteristics of the integrated circuit devices to those of the AN/UYK-1 hardware. A photograph of this simulator is shown in figure 1.

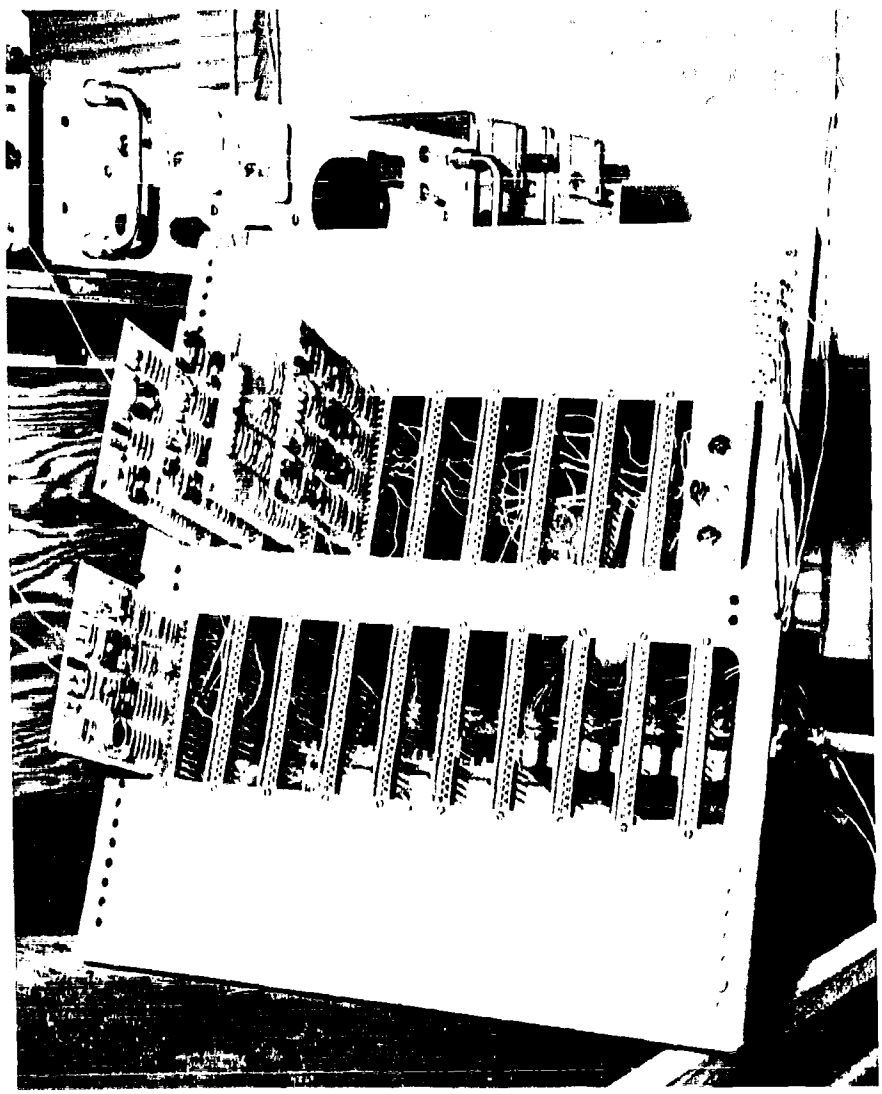


Figure 1. State counter simulator, showing cordwood level-changing circuits and AN/UYK-1 logic cards.

In the AN/UYK-1, the three state counter flip-flops are driven by various logic signals generated within the computer itself. In the simulator, the three flip-flops are wired as a counter to reproduce typical logic functions of the state counter. The simulator logic was written to cause the counter to generate in sequence the following AN/UYK-1 commands: 001, 011, 000, 010, 101, and 111. These commands correspond to READ LOGAND, WRITE LOGAND, READ INDIRECT ADDRESS, WRITE INDIRECT ADDRESS, EXECUTE PRIMARY COMMAND, and WRITE OPERAND.

Figure 2 is a block diagram of the simulator. The blocks designated "Q" are AN/UYK-1 R-S flip-flops, and the symbols labeled "D" are AN/UYK-1 AND/OR gates. In order to generate the commands indicated above, these circuit elements are connected as a counter whose present state is a function of its previous state. In addition to providing a source of driving signals, the flip-flop output waveforms may also be sampled for comparison purposes.

The components labeled "L" on the diagram are level changers. These circuits are encapsulated cordwood modules which use standard components. Level-changing circuits are required to convert the logic levels of the AN/UYK-1 (0 to -13 volts) to those of the integrated circuits (0 to +3 volts). Both normal and complemented signals are available at the output of the level changers for driving the integrated circuit modules.

As shown on the diagram, two AN/UYK-1 cards (clock oscillator and amplifier) were required to provide the proper clock pulses for the simulator. These clock pulses are also available for derivation of clock pulses usable with the integrated circuit devices.

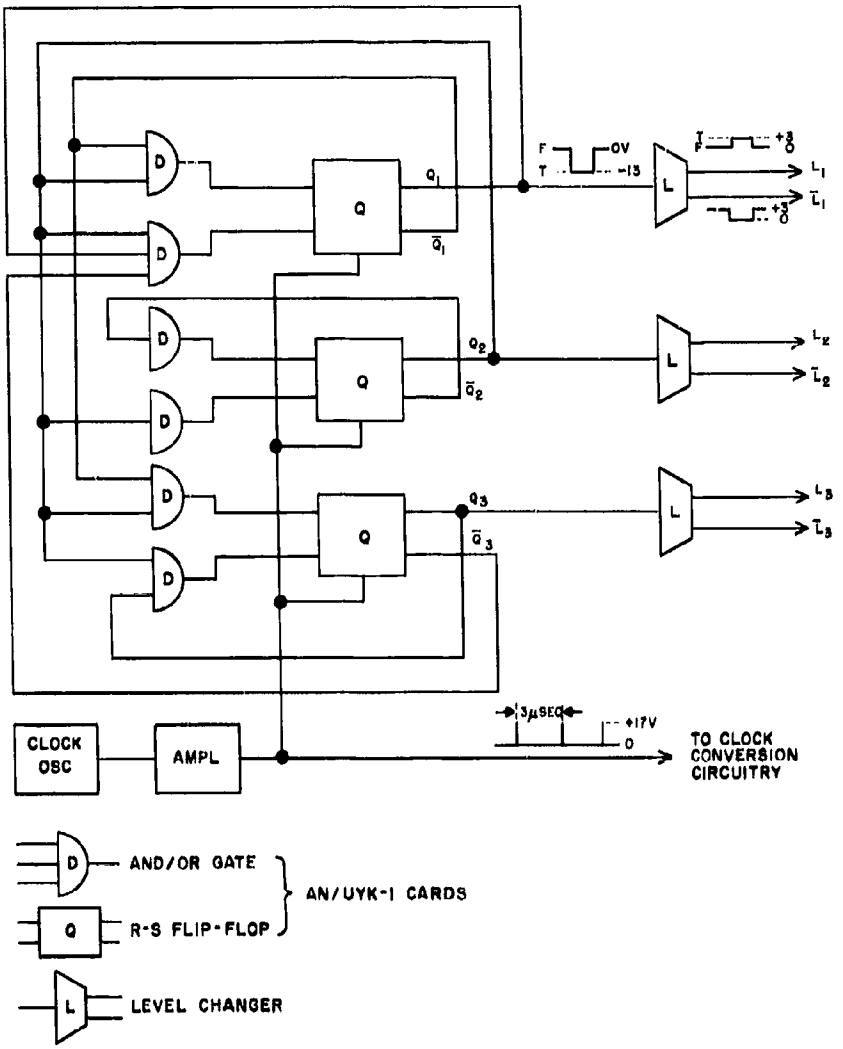


Figure 2. AN/UYK-1 state counter simulator.

INTEGRATED CIRCUIT STUDY

Study of the use of integrated circuit devices to duplicate functionally the AN/UYK-1 state counter and the R-S flip-flop card involved the products of several manufacturers. The methods used and the results obtained are given below.

FAIRCHILD MICROLOGIC ELEMENTS

Fairchild Semiconductor produces a family of high-speed, low-power Micrologic elements for use in digital systems. These elements employ Direct-Coupled Transistor Logic (DCTL) NOR circuitry and operate at speeds in excess of 1 Mc/s. They are packaged in TO-5 headers, dissipate an average power of 30 mw, and operate over a temperature range of -55°C to +125°C. Figure 3 is a photomicrograph of a Fairchild flip-flop element showing connection of the diffused device to pins on a TO-5 header.

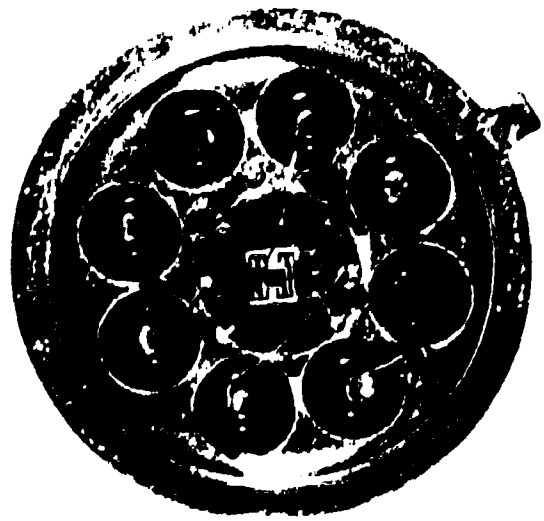


Figure 3. Photomicrograph of Fairchild flip-flop element.

The block diagram of figure 4 illustrates the manner in which the state counter functions were implemented with Fairchild Micrologic devices. The blocks designated "F" are Micrologic flip-flops; the symbols labeled "G" are Micrologic NOR gates; and the circles labeled "B" are Micrologic buffers.

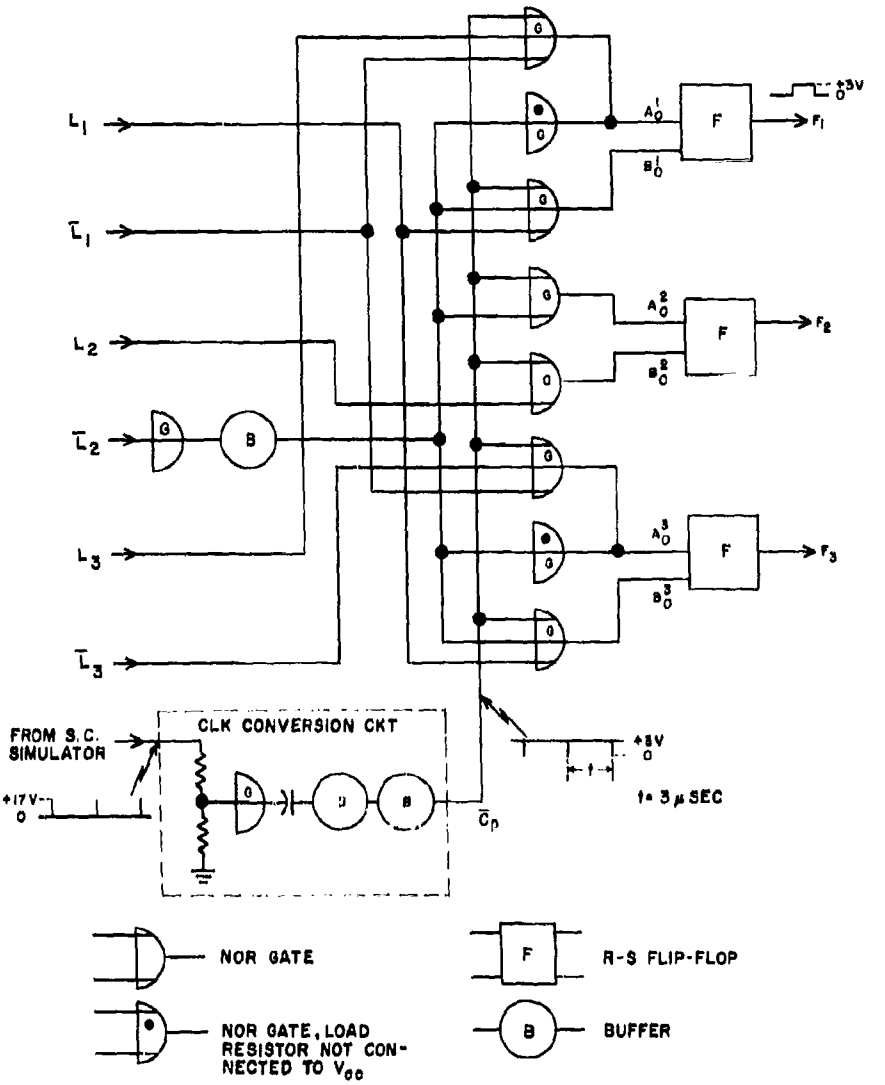


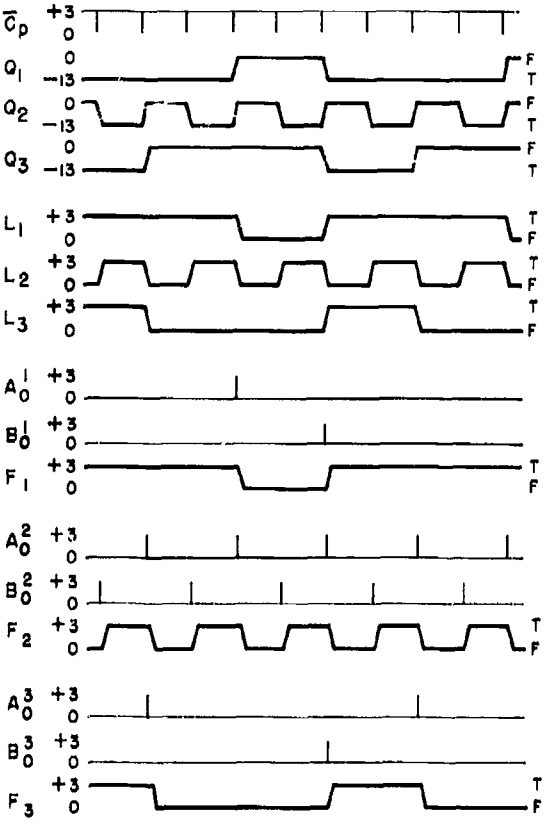
Figure 4. Implementation of state counter with Fairchild elements.

The "G" and "B" elements and associated standard components shown within the dashed block convert the AN/UYK-1 clock pulses to a form usable with the Fairchild elements. In this case, a "G" element is used to invert the attenuated AN/UYK-1 clock pulse. The signal is then differentiated and inverted by the first "B" element, and a second "B" element is required to re-invert the signal and drive the clock-pulse lines.

The normal and complemented outputs of the simulator are used to represent state counter input signals which in the actual computer are generated by the logic section. These signals are applied to the Fairchild gates to cause the flip-flops to change state in accord with certain input signal combinations. The logic is such that the Fairchild state counter changes state in step with the simulator for ease of waveform comparison.

A "B" element is also used to bolster driving signal $\overline{L}_2$ because this particular signal drives a large number of gates. The "G" element compensates for unwanted inversion through the "B" element.

The timing diagram and equations associated with the block diagrams of figures 2 and 4 are shown in figure 5. The clock output $\overline{C}_p$ is a negative-going, 3-volt pulse occurring at 3-microsecond intervals. The normal outputs (Q_1, Q_2, and Q_3) of the simulator flip-flops are logic levels of zero (false) and -13 volts (true). The normal outputs of each level changer are L_1, L_2, and L_3. At this point, zero volts is a false signal and +3 volts is a true one. The input signals to the "F" elements (A_0^1, B_0^1, etc.) correspond to the notation on the block diagram in figure 4. The "F" element outputs are F_1, F_2, and F_3. Figure 5 also lists the logic equations which define the operation of the Fairchild-implemented state counter, and indicates the implementation of the counter with complemented inputs as required to obtain an AND function with NOR logic gates.



TIMING DIAGRAM (NOT TO SCALE)

NOTE: BECAUSE THE FAIRCHILD GATE ELEMENT UTILIZES *NOR* LOGIC, IT IS NECESSARY TO IMPLEMENT THE GATE WITH THE COMPLEMENT OF EACH INPUT SIGNAL TO OBTAIN THE *AND* FUNCTION.

Figure 5. Timing diagram and equations for Fairchild implementation of the state counter.

Figure 6 shows the rear of the simulator with the Fairchild Micrologic elements mounted on part-boards below. The long strip contains principally "B" elements and clock-pulse circuitry, while the shorter boards contain mainly "G" and "F" elements. Figure 7 is a closeup of the Micrologic breadboard showing the TO-5 cans.

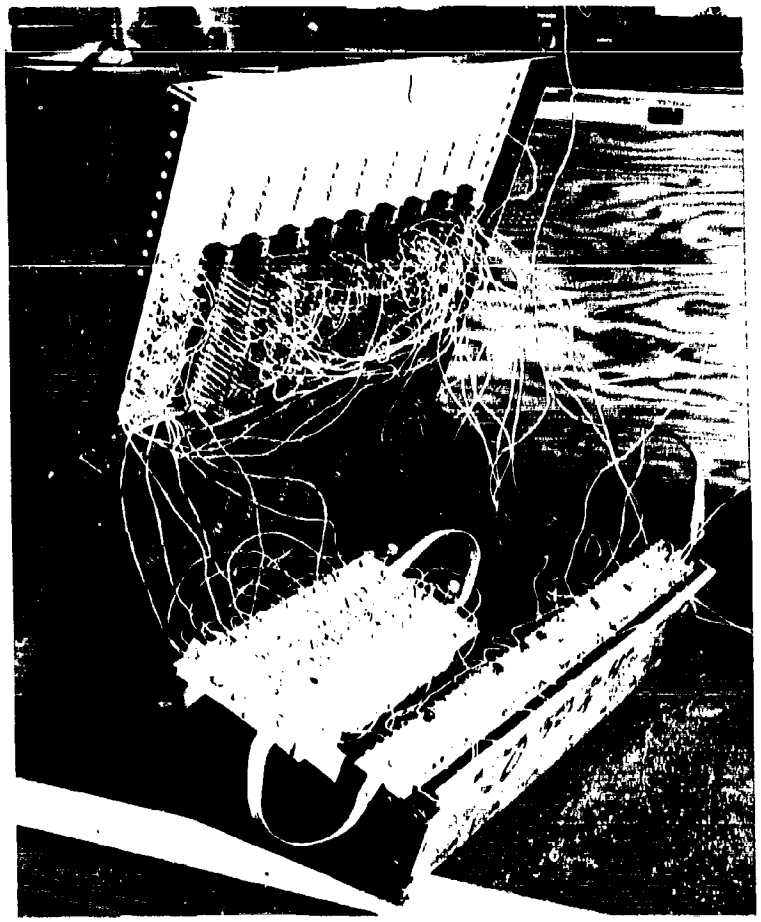


Figure 6. Fairchild breadboard of state counter circuit, mounted on rear of simulator chassis.

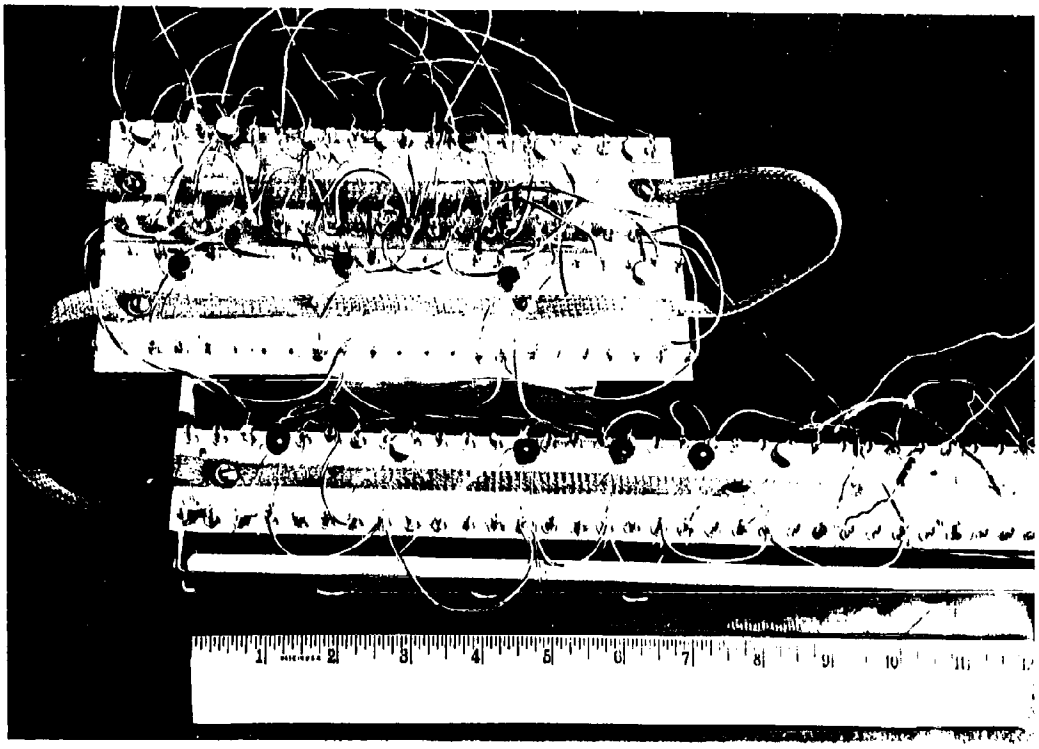


Figure 7. Closeup of Fairchild breadboard showing TO-5 headers.

Figure 8 is a photograph of the AN/UYK-1 and Fairchild clock waveforms. Figure 9 shows the outputs of the "Q" flip-flops. This photograph is aligned with figure 8 to indicate timing in relation to clock pulses. Figure 10 shows the output signals of the "F" flip-flops. The comparatively fast rise-times of the Fairchild elements are quite evident.

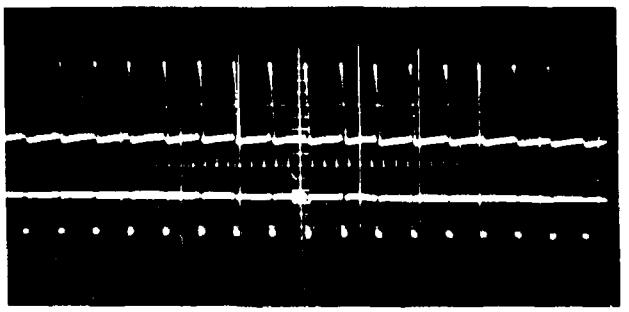


Figure 8. AN/UYK-1 and Fairchild clock waveforms. Top trace is AN/UYK-1 clock with vertical sensitivity of 20 v/cm. Bottom trace is Fairchild clock with vertical sensitivity of 2 v/cm. Sweep speed is 5 μsec/cm.

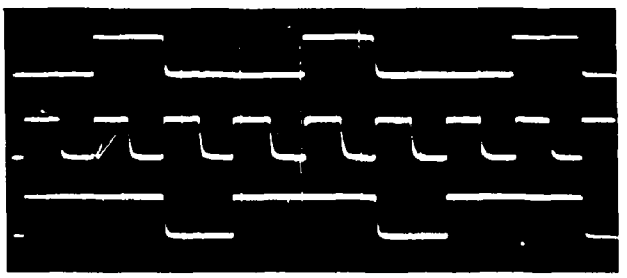


Figure 9. AN/UYK-1 flip-flop output waveforms. Signals are Q_1, Q_2, and Q_3 from top. Vertical sensitivity is 20 v/cm. sweep speed is 5 μsec/cm, and signal amplitude is 0 to -13 volts.

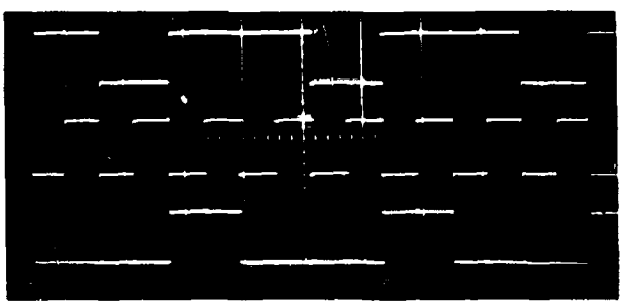


Figure 10. Fairchild flip-flop output waveforms. Signals are F_1, F_2, and F_3 from top. Vertical sensitivity is 1 v/cm. sweep speed is 5 μsec/cm. and signal amplitude is 0 to +0.8 volt.

Studies of performance of the Fairchild elements with regard to voltage levels were made by varying supply voltages on the gate (G) and flip-flop (F) elements and noting the limits of voltage variation at which improper operation resulted. The supply voltage applied to the "G" elements could be lowered from its normal level of +3 volts to about 1 volt before improper operation of the element resulted, while the "F" elements ceased to function properly when the supply voltage was lowered to 1.2 volts: a variation of 1.8 volts from the normal +3 volt level. Operation was not disturbed even at these lower levels by noise or pickup on the breadboard layout used. Increases in the supply voltage on the "F" and "G" elements indicated that an increase of 200 or 300 per cent in the rated voltage produced no particular adverse effects other than increased heat dissipation. While no extensive life-test data were taken on these elements using a duty cycle typical of AN/UYK-1 operation, it appeared that variations in the supply voltages of ±60 per cent could easily be tolerated before unreliable operation of the elements would occur.

Further studies were made to determine the magnitude of logic signals which must be maintained to insure reliability. The input signal to a "G" element can fall to a level of 0.5 volt before the element ceases to function correctly, while the input to an "F" element can be lowered to a level of 0.8 volt before improper operation begins. Input voltages of this magnitude approach the V_{BE} turn-on voltage level below which the transistors cannot be switched. In general, if the logic signals are supplied by Micrologic elements, the amplitude of these signals will depend upon the extent to which the driving elements are loaded. Fan-out on these elements is defined in terms of the number of Micrologic loads to be driven. The manufacturer specifications state that a "G" element should be capable of driving five Micrologic loads. Investigation revealed that a "G" element output is about 1.5 volts when one load is being driven, and falls to 1.1 volts when driving five loads. These levels are well above the 0.5 and 0.8 volt levels discussed above. If an element is required to drive more than five loads, "B" or buffer elements, which are

specified as capable of driving 25 Micrologic loads, are available.

In addition to the work described above, a specific individual logic element of the AN/UYK-1, the R-S flip-flop, was reproduced functionally for study. The conventional AN/UYK-1 R-S flip-flop card contains two flip-flops and their associated neon-lamp circuits. This card was duplicated, with the exception of the lamp circuits, using Fairchild elements and appropriate level changers to check its operation as a direct replacement in the AN/UYK-1 cabinet. Figure 11 shows the arrangement of the components on this card. The four encapsulated cordwood modules are input level changers. The four unencapsulated units are output level changers. The three Micrologic elements adjacent to the output level changers are one "G" and two "B" elements comprising the clock-conversion circuit. The other two are "S" elements. The four potentiometers provide bias adjustment for the output level changers. The two unused sockets, not utilized in the implementation of the R-S flip-flops, will be covered in a subsequent discussion of the delay flip-flop card. Figure 12 shows the reverse side of the card.

Figure 13 is a functional block diagram of the R-S flip-flop card in Micrologic form. Normal signals from an AN/UYK-1 gate are fed into level changers and thence into "S" half-shift register elements (in dotted squares). The outputs of the elements are changed back to AN/UYK-1 logic levels and fed to AN/UYK-1 gates. "S" elements are used because they consist of two two-input gates and a flip-flop on a single header and because the inputs are limited to single signals plus clock. An "S" element is in this case a convenient functional replacement for an R-S flip-flop. It should be noted that in figure 4 the combination of the two middle Micrologic "G" gates and the "F" element which they drive can be replaced by a single "S" element. When these "G" and "F" elements were replaced in the circuit of figure 4 by a single "S" element, performance was unchanged from that of the original configuration. The Micrologic R-S flip-flop card of figure 11 was used

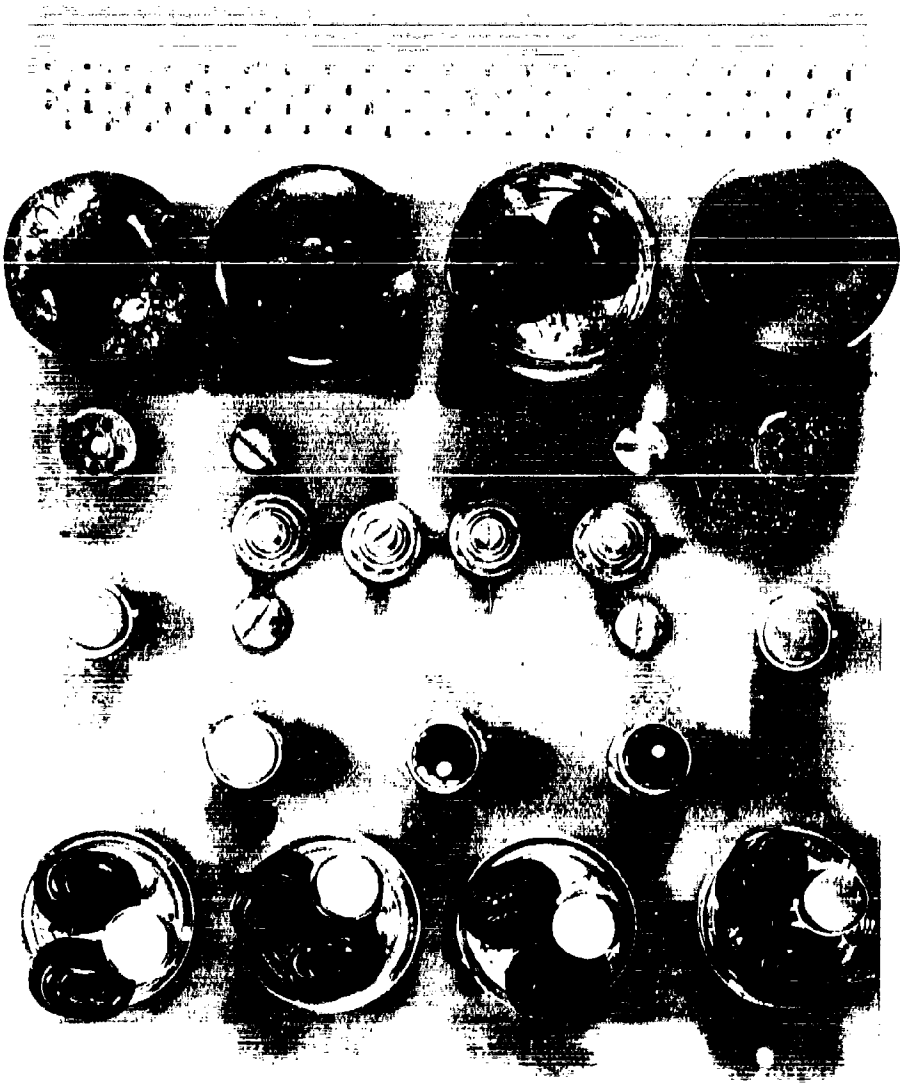


Figure 11. R-S flip-flop card, showing Fairchild elements and level-changing circuit.

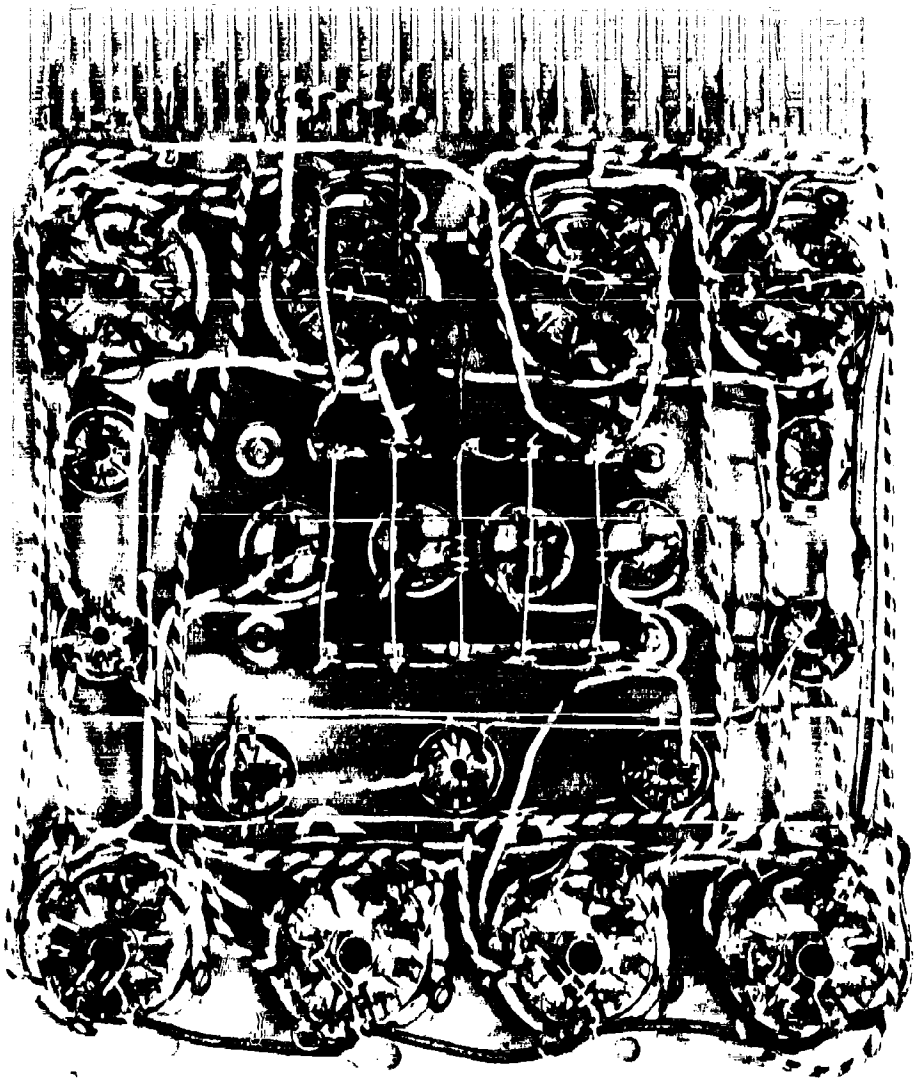


Figure 12. R-S flip-flop card wiring.

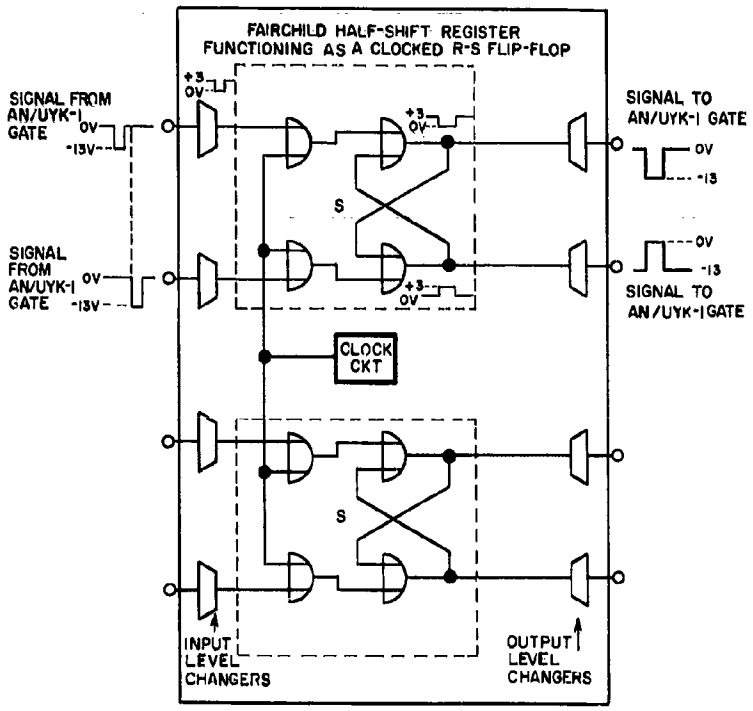


Figure 13. Implementation of R-S flip-flop card with Fairchild Micrologic elements.

successively to replace several of the flip-flop cards in the AN/UYK-1 cabinet and operated very successfully in each case. Obviously, level changers would not be necessary if the entire circuit were implemented initially in low-level logic.

An AN/UYK-1 card used even more extensively than the R-S flip-flop, the delay flip-flop, was also implemented with Micrologic elements simply by altering the R-S flip-flop circuit board. This was accomplished by adding two "G" elements (one per flip-flop circuit, inserted in the two unused sockets previously mentioned) and small wiring

changes. Figure 14 shows the manner in which the Micrologic devices were connected to perform the delay flip-flop functions. This delay flip-flop card was also successfully tested in the AN/UYK-1 cabinet.

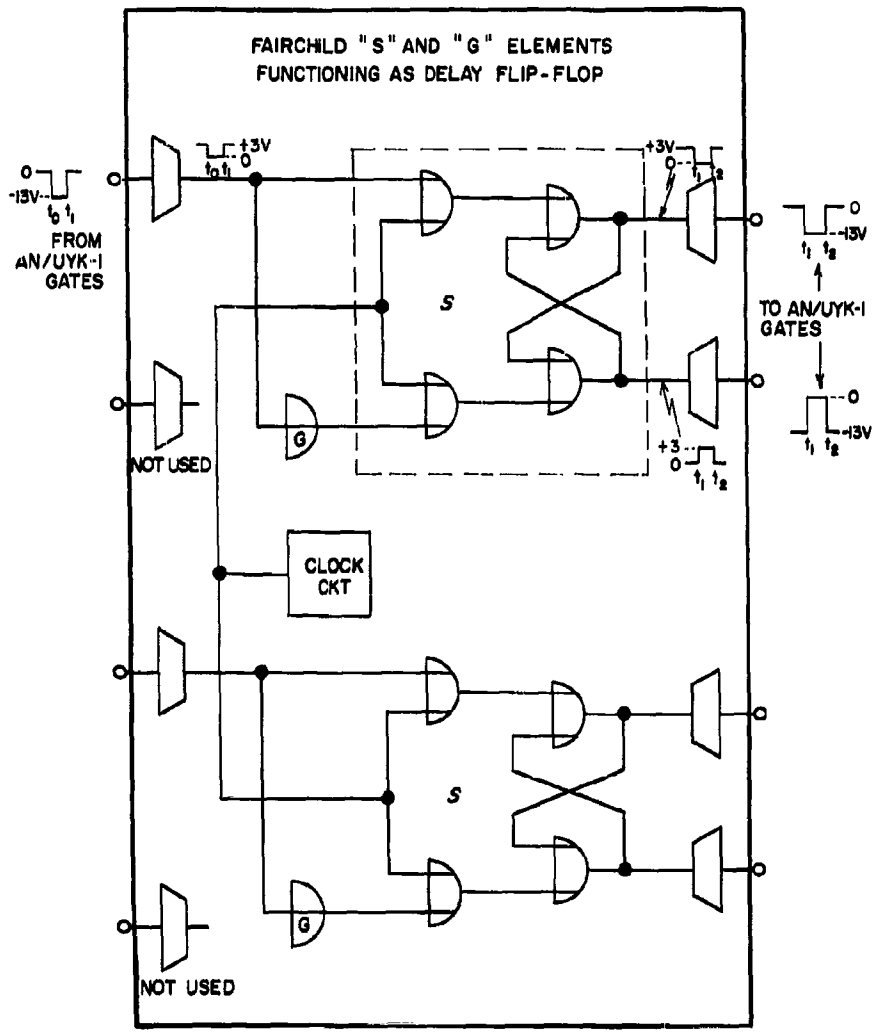


Figure 14. Implementation of delay flip-flop card with Fairchild Micrologic elements.

Some indication of the cost of Fairchild Micrologic elements can be obtained from purchasing experience. Early in the problem the price was $120 each for comparatively small quantities of "F," "S," "B," "C," "H," and "G" elements. Early in calendar 1962 the price of several elements was reduced, for the "F" element to $85 and for the "G" element to $65. A further reduction became effective 1 June 1962, when the cost of the "F" element dropped to $74.50 and that of the "G" element to $52.50. Reductions were also made in the cost of other elements. A further saving may be realized with the purchase of quantities in excess of 100: For example, the "F" elements can now be purchased for $49.90 each in quantities of 100 or more.

TEXAS INSTRUMENTS SERIES-51 SEMICONDUCTOR NETWORKS

The second type of integrated circuitry investigated was the Series-51 Semiconductor Networks marketed by Texas Instruments (TI). These devices employ Resistor-Capacitor-Transistor Logic (RCTL) NOR/NAND circuits. Their average power dissipation is 4 mw per logic network and their operating temperature range is between -55°C and +125°C. Figure 15 shows a TI package mounted in the center of a test holder.

Prior to the feasibility study related to the AN/UYK-1 computer, several observations were made regarding TI elements in general and the results were compared with specifications recorded on company data sheets. Delay and rise times in many cases were found to be in excess of those specified. These deficiencies were not objectionable at the comparatively low AN/UYK-1 clock rate of 0.3 Mc/s, but might prevent the operation of a system at slightly higher frequencies.

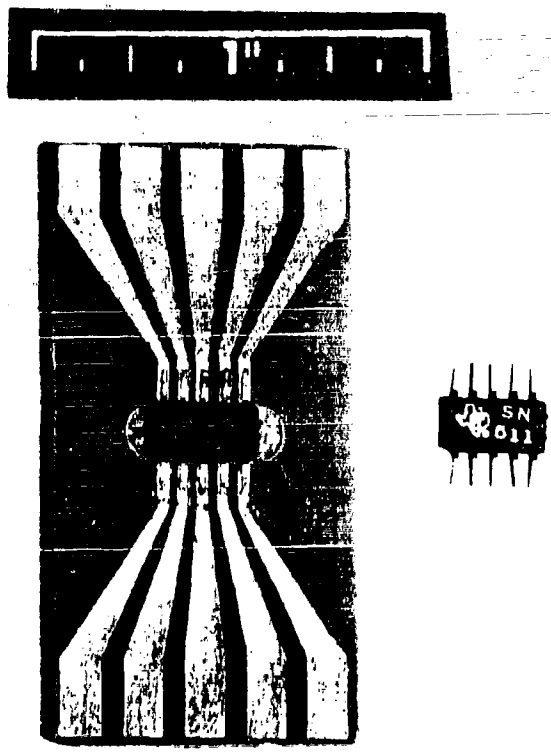


Figure 15. Texas Instruments Series-51 Semiconductor Network, mounted and unmounted.

The AN/UYK-1 state counter was implemented functionally with TI components in a manner similar to that described for the Fairchild elements. Figure 16 is a photograph of the TI-implemented state counter and figure 17 illustrates the manner in which the TI networks were connected. In figure 17, the blocks designated "T" are SN511 flip-flop networks and the symbols labeled "G" are one-half of an SN514 dual gate. The block labeled CLOCK CONVERSION CKT represents circuitry that was designed to convert the AN/UYK-1 clock pulse to one compatible with the TI devices.

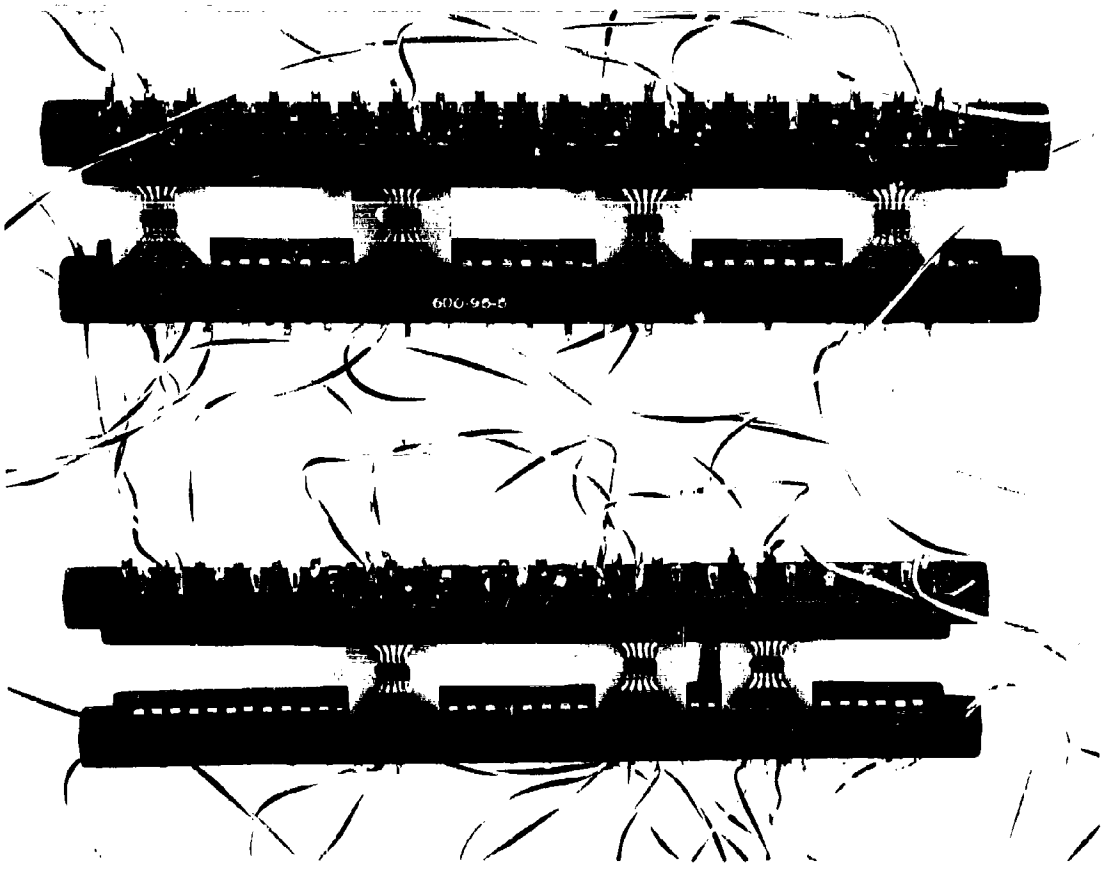


Figure 16. State counter, Texas Instruments implementation.

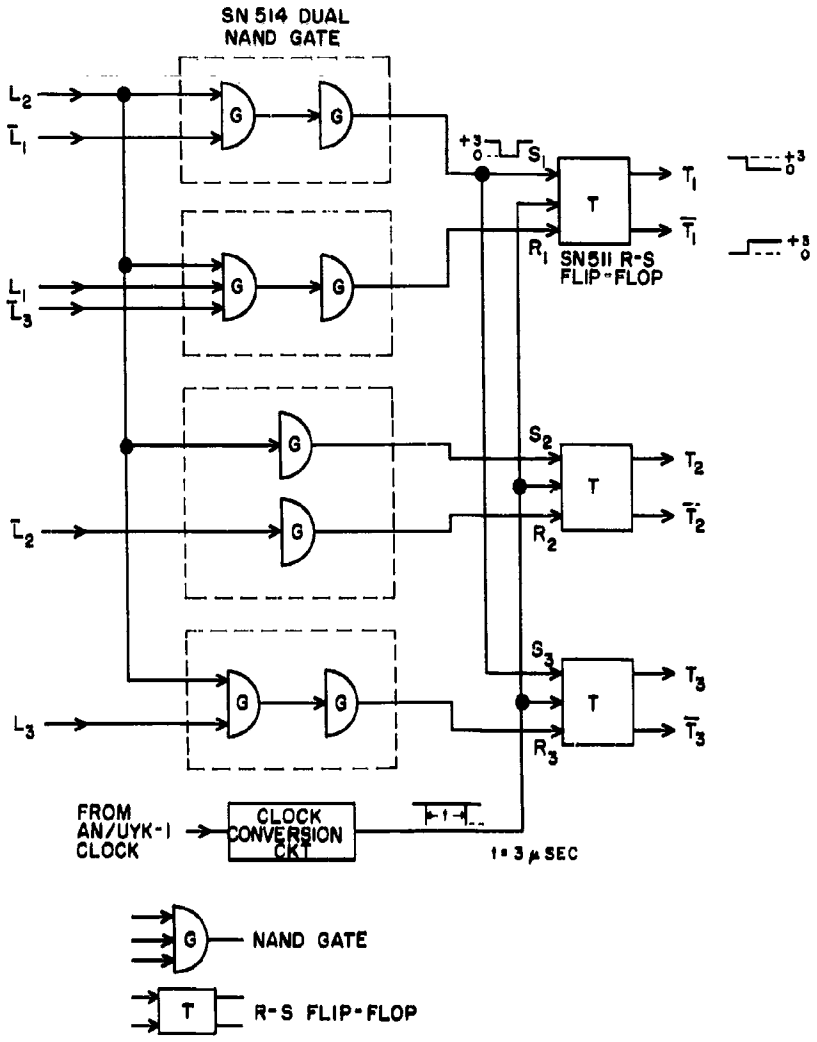
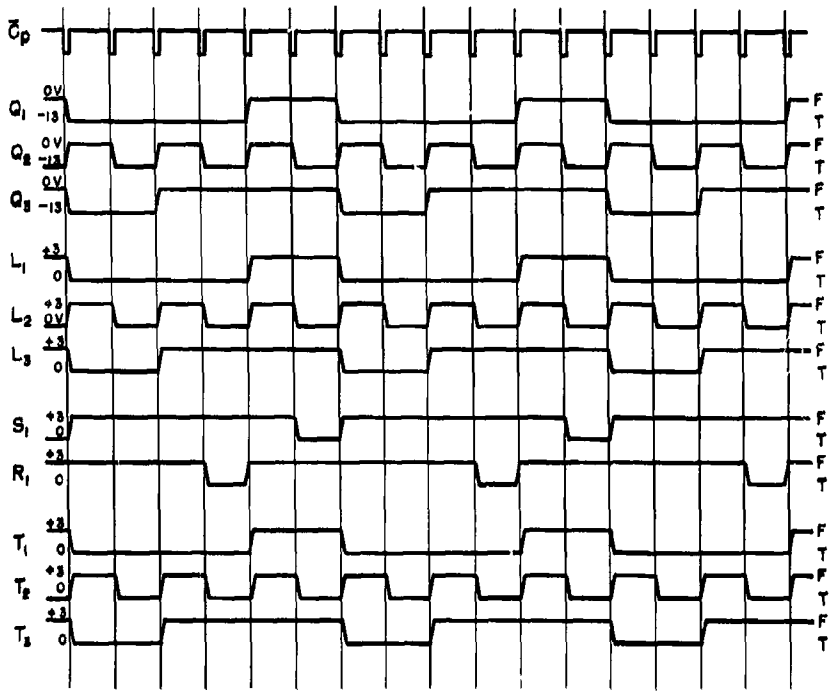


Figure 17. Implementation of state counter with Texas Instruments elements.

Figure 18 is the timing diagram associated with the circuit of figure 17. The signals labeled L_1, L_2, and L_3 are provided by the state counter simulator. The clock signal is the output of the clock conversion circuitry. Set and reset inputs are shown for the first flip-flop only.



LOGIC EQUATIONS

$S_1 = \bar{L}_1 L_2$ $\quad R_1 = L_1 L_2 \bar{L}_3$

$S_2 = \bar{L}_2$ $\quad R_2 = L_2$

$S_3 = \bar{L}_1 L_2$ $\quad R_3 = L_2 L_3$

Figure 18. Timing diagram and equations for Texas Instruments implementation of the state counter.

Signals T_1, T_2, and T_3 are the outputs of the TI flip-flop elements. Unlike the Fairchild element implementation, a negative logic convention, in which zero volts corresponds to true and +3 volts to false, was adopted for use with the TI devices.

Figures 19, 20 and 21 are photographs of voltage waveforms as seen at various points in the circuit of figure 17. The top trace of figure 19 is the AN/UYK-1 clock pulse. Immediately below is the output of the clock-conversion unit that is applied to the TI flip-flop devices. The three waveforms shown in figure 20 are the outputs of the AN/UYK-1 state counter flip-flops and represent the sequence through which the state counter steps. After suitable level changing, these signals are applied to the TI gate networks. The three waveforms of figure 21 are the outputs of the TI flip-flop devices. Although long rise and fall times are evident, the logic sequence of the state counter is seen to be faithfully reproduced.

An investigation was made to determine the amount of reduction in the V_{cc} of a gate that would cause the output waveform of that gate to deteriorate to a point where it would no longer drive the required number of loads or where the waveform was so distorted that it could no longer be considered a proper logic signal. In this and subsequent tests increases in supply voltage (within reasonable limits) caused no adverse effects. All discussions regarding voltage performance tests are therefore confined to voltage reductions. All tests were made using the AN/UYK-1 clock rate.

The logic input of the SN514 gate under test, obtained from one of the flip-flops that comprise the state counter, was monitored throughout the test and no noticeable deviations were observed. The output of the SN514 gate was connected to five input terminals of a SN512 gate to provide a "worst case" loading condition.

When the V_{cc} of the driving gate was lowered 60 per cent (to 1.2 volts from a normal of 3 volts) the output of

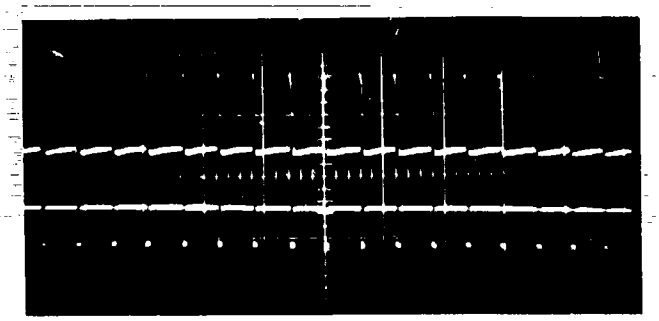


Figure 19. AN/UYK-1 and Texas Instruments clock waveforms. Top trace is AN/UYK-1 clock with vertical sensitivity of 20 v/cm. Bottom trace is Texas Instruments clock with vertical sensitivity of 2 v/cm. Sweep speed is 5 μsec/cm.

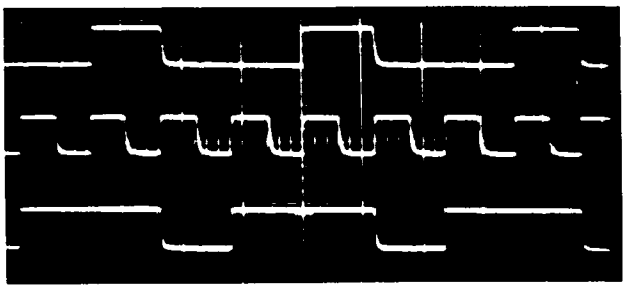


Figure 20. AN/UYK-1 flip-flop output waveforms. Signals are Q_1, Q_2, and Q_3 from top. Vertical sensitivity is 20 v/cm, sweep speed is 5 μsec/cm, and signal amplitude is 0 to -13 volts.

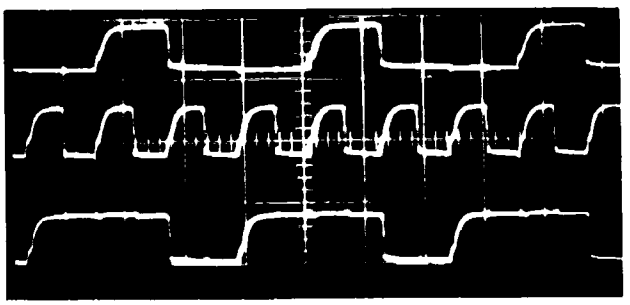


Figure 21. Texas Instruments flip-flop output waveforms. Signals are T_1, T_2, and T_3 from top. Vertical sensitivity is 2 v/cm, sweep speed is 5 μsec/cm, and signal amplitude is 0 to +1.6 volts.

the gate was reduced to 0.8 volt from a normal of 1.8 volts. A further reduction resulted in a signal which was of sufficient amplitude to turn on the driven elements but not to drive them into saturation fast enough to produce a proper logic level output.

A similar test was made on the SN511 flip-flop element. In this instance the output was connected to four logic loads. When the flip-flop V_{cc} was reduced to 2.1 volts from a normal of 3 volts, the element became inoperative. This test indicated that a reduction in V_{cc} of up to 30 per cent may be tolerated. Since V_{cc} is common to both gates and flip-flops, this figure then defines the lower limit of the system power supply fluctuation.

TI elements were also employed to duplicate functionally the AN/UYK-1 R-S flip-flop card. This R-S flip-flop is shown in figure 22 in block diagram form. Figures 23 and 24 are photographs of the card itself. Because the level-changing and clock-pulse circuitry designed for use with the Fairchild devices was found to work satisfactorily with the TI units, the R-S flip-flop card originally constructed was simply altered slightly so that the same function could be performed using the TI Semiconductor Network devices. The TI card was substituted for various AN/UYK-1 R-S flip-flop cards in the computer cabinet with complete success.

The cost of the TI Semiconductor Networks at the start of the project in early calendar 1962 was $115 for the flip-flop element and $95 for the gate element, when purchased in small lots. As of 5 June 1962, the price of a flip-flop element was $80 when purchased in small quantities and as low as $53 in quantities of 251 or more, while the price of the gate element was $70 in small lots and $47 in larger lots.

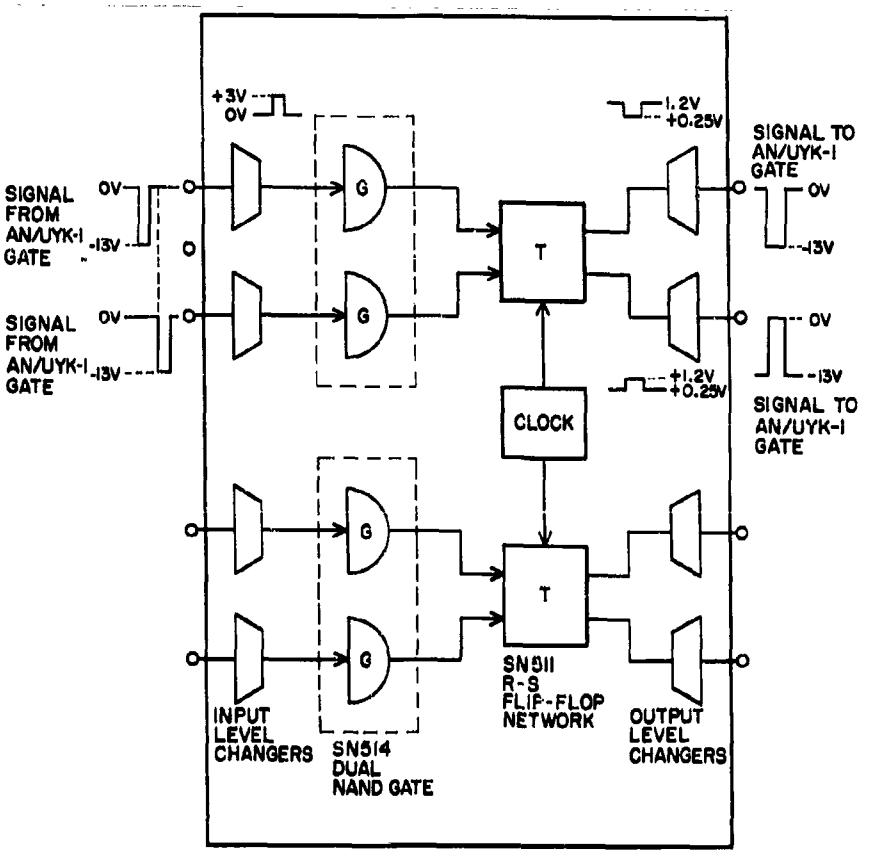


Figure 22. Implementation of R-S flip-flop card with Texas Instruments elements.

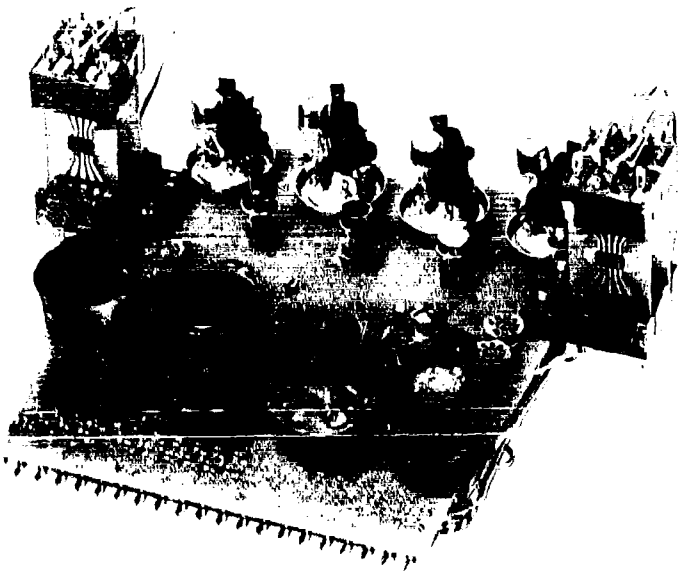


Figure 23. R-S flip-flop card, showing addition of Texas Instruments Semiconductor Network elements.

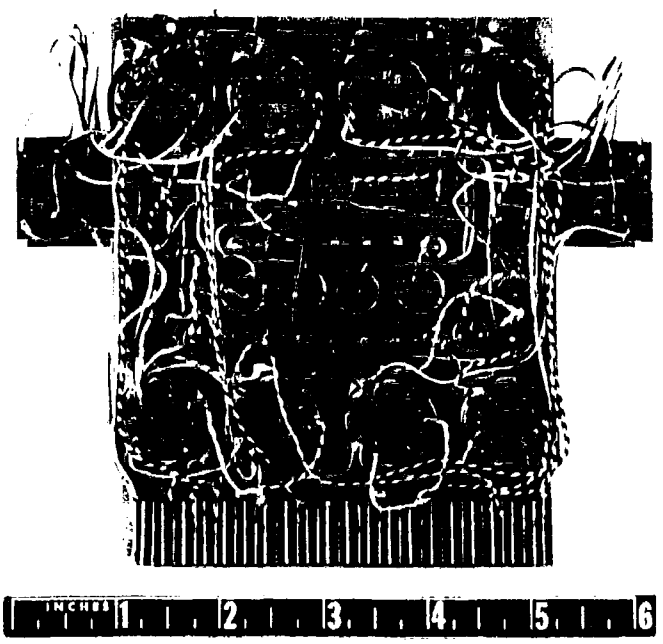


Figure 24. R-S flip-flop card, Texas Instruments implementation wiring.

GENERAL INSTRUMENTS NANOCIRCUITS

General Instruments (GI) Corporation has developed microelectronic silicon Nanocircuits operating at and above 15 Mc/s with a maximum power dissipation of 80 to 85 mw and rise and fall times of 12 to 30 nanoseconds. These elements, packaged on TO-5 headers, are specified to operate in a temperature range of -55°C to +125°C. Three separate supply voltages (V_{cc} collector supply voltage, V_{cl} clamping voltage, and V_{bb} gate bias voltage) are required. In addition, two elements, NC-9 (steering gate) and NC-8C (flip-flop), are used to perform the flip-flop function. These units employ DRT (Diode-Resistor-Transistor) logic. The logic levels are +0.3 and +4.0 volts.

Figure 25 shows the manner in which these units were employed to reproduce functionally the AN/UYK-1 state counter. The blocks labeled "GF" are NC-8C flip-flop elements and the blocks labeled "SG" are NC-9 flip-flop steering gates. The block labeled "C" represents circuitry designed to convert the AN/UYK-1 clock to the proper logic levels required by these units.

The steering gate preceding the flip-flop causes it to change state on the trailing edge of the clock pulse, precluding the necessity of a two-phase clock in cases (such as shift registers) where the input to a flip-flop might be driven by the output of another flip-flop.

Figure 26 shows the timing diagram and equations associated with the circuit of figure 25. Included in this figure are the outputs of the state counter simulator (L_1, L_2, and L_3); the outputs of the GI flip-flop elements (GF_1, GF_2, and GF_3); the output of the clock conversion circuit, $\overline{C}_p$; and the set and reset inputs to the first flip-flop, S_1 and R_1.

Figure 27 shows the GI-implemented state counter with the GI elements mounted on parts boards at the rear of the state counter simulator.

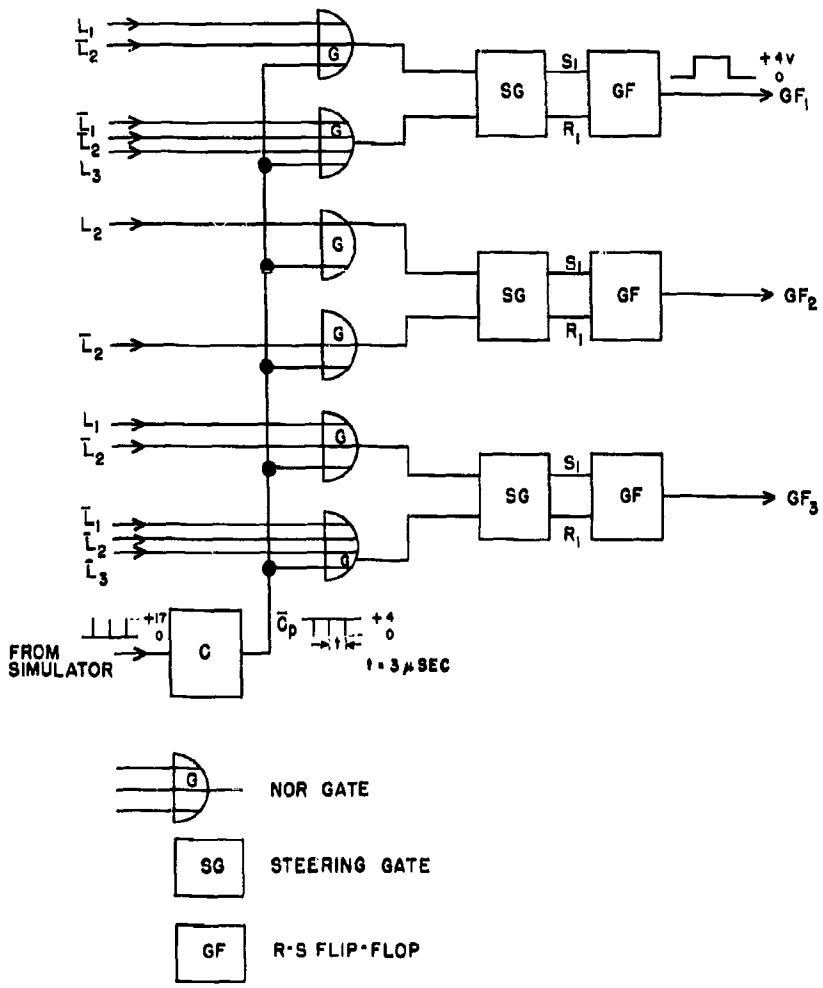


Figure 25. Implementation of state counter with General Instruments elements.

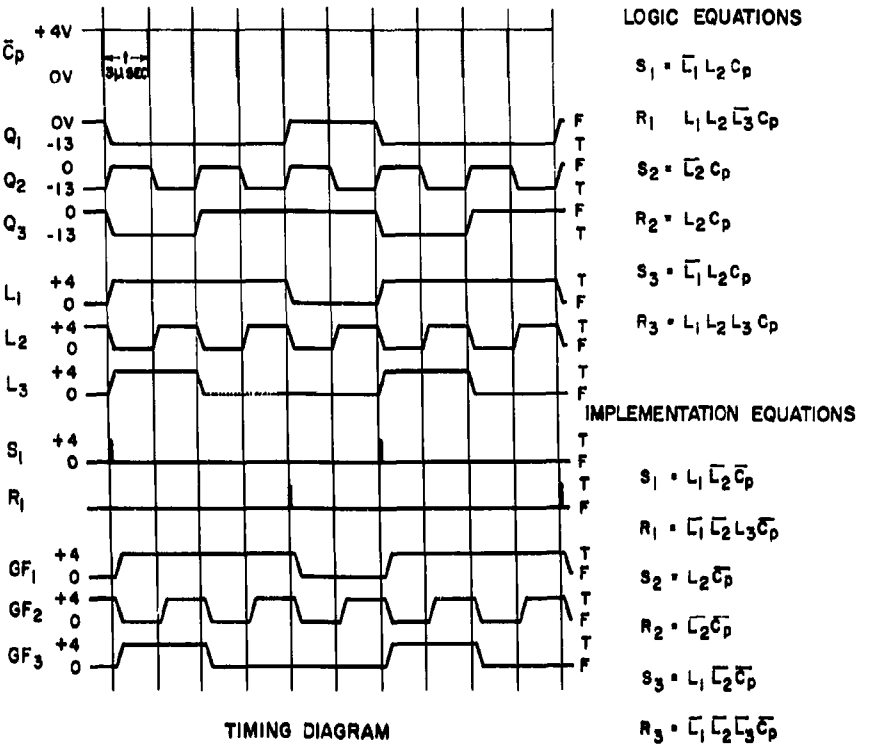


Figure 26. Timing diagram and equations for General Instruments implementation of the state counter.

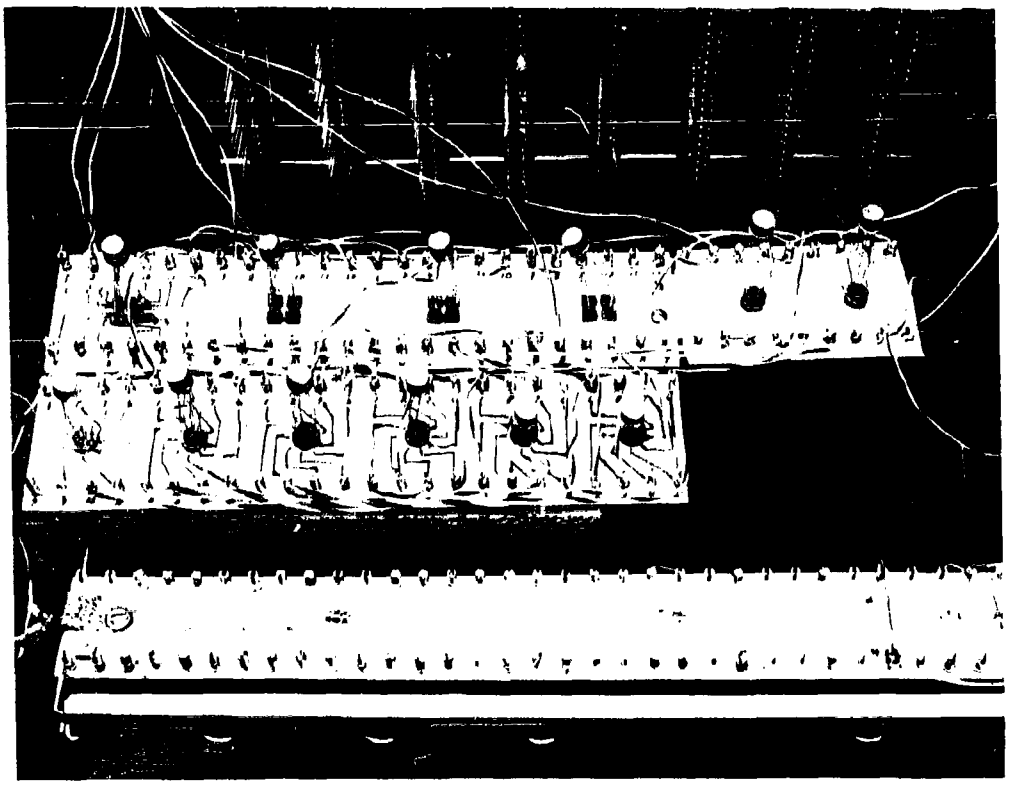


Figure 27. State counter, General Instruments implementation.

Figure 28 is a photograph of the AN/UYK-1 and GI clock waveforms. Note that the GI clock has the same configuration as the Fairchild clock. Figure 29 shows the outputs of the "Q" flip-flops for comparison with the outputs of the GI flip-flops which appear in figure 30 immediately below. The three figures are aligned vertically to show the timing relationship to the clock pulses. If it is remembered that for the Q outputs a -13, or low voltage as it appears in the waveforms, is a true logic level while a high voltage is a true level for the GF outputs, it is apparent that the GI flip-flops follow the AN/UYK-1 state counter logic sequence. Also note that the GI flip-flop outputs are at least 4 volts in magnitude with extremely fast rise and fall times.

Tests were made on the GI elements to determine their ability to produce usable outputs when each of the supply voltages was reduced from normal value. A usable output was defined as one that would cause the element or elements being driven to switch or change state, and one whose logic identity was not destroyed by increased rise and fall times.

Observations revealed that while the flip-flop element would respond to an input signal of 0.7 volt in magnitude and 20 nanoseconds fall time, a gate would cease to operate with an input of less than 2.5 volts. This indicated that the value of any one supply voltage for which the logical gate signals were reduced to 2.5 volts was the allowable limit for that particular supply voltage variation.

The V_{cc} (+8 volts) applied to the flip-flop elements was lowered to 5.5 volts (31 per cent), and that applied to the gate elements to 2.5 volts (68 per cent) before the outputs of the elements dropped to 2.5 volts; the V_{cl} (+3.2 volts) was reduced to 1.8 volts (44 per cent) on the flip-flops and to 2.0 volts (37 per cent) on the gate elements, before the outputs fell to 2.5 volts. Thus the allowable variation of V_{cc} was 31 per cent and that of V_{cl} was 37 per cent. Reductions of V_{bb} (-3.0 volts) did not have any appreciable effect on the amplitude of the gate output. All of the above tests were made under the worst-case conditions: a fan-out of four.

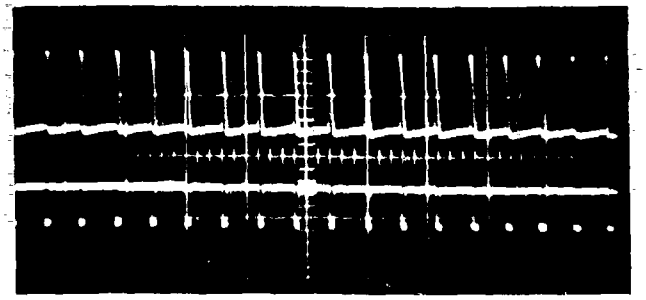


Figure 28. AN/UYK-1 and General Instruments clock waveforms. Top trace is AN/UYK-1 clock with vertical sensitivity of 20 v/cm. Bottom trace is General Instruments clock with vertical sensitivity of 2 v/cm. Sweep speed is 5 μsec/cm.

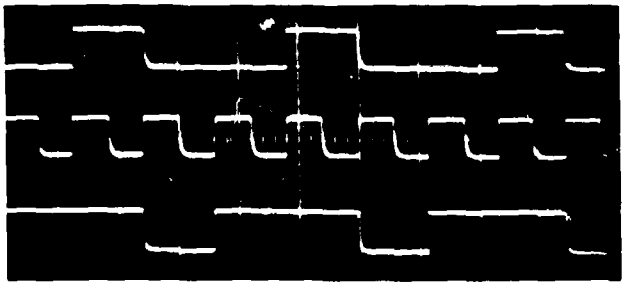


Figure 29. AN/UYK-1 flip-flop outputs. Signals are Q_1, Q_2, and Q_3 from top. Vertical sensitivity is 20 v/cm, sweep speed is 5 μsec/cm, and signal amplitude is 0 to -13 volts.

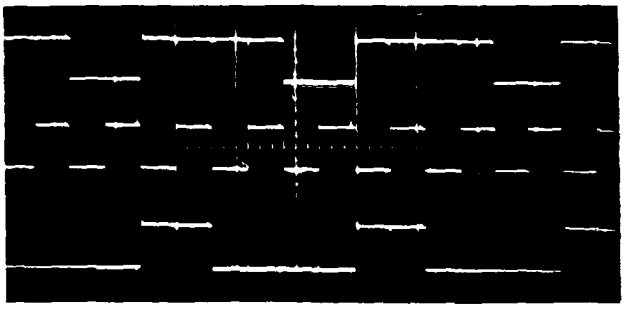


Figure 30. General Instruments flip-flop outputs. Signals are FG_1, FG_2, and FG_3 from top. Vertical sensitivity is 5 v/cm, sweep speed is 5 μsec/cm, and signal amplitude is 0 to +4 volts.

The implementation of the R-S flip-flop card was not undertaken with the GI Nanocircuits. Observations of the performance of the Nanocircuits in the state counter implementation led to the conclusion that successful operation could be expected and that the additional information gained, if any, would not warrant the time and effort involved in constructing such a card.

A purchase of GI elements was made in May 1962 and the cost per element, regardless of type, was $75.

DATA TRANSMISSION AND MEMORY ACCESSION

The implementation of the state counter and R-S flip-flop functions as reported above necessitated the use of level-changing circuitry to convert the driving signals of AN/UYK-1 logic voltage levels to those of the integrated circuit devices. If the entire logic portion of the AN/UYK-1 were to be constructed with integrated circuit elements, no level changers would be required between circuits within the logic section but level-changing and/or driving circuitry would be needed between the logic section and peripheral equipment. This need arises because peripheral equipment may or may not utilize zero-to-plus-3-volt logic signals, and may occasionally be connected to the computer by relatively long lines requiring a high signal-to-noise ratio for reliable data transmission. In addition, the integrated circuit devices tested perform logic functions only; memory accession requires analog pulse-shaping and driving circuits which cannot at present be constructed with miniaturized integrated devices.

The requirement of input/output level-changing and driving circuits, also common to computers using conventional circuitry, cannot be met using the microelectronic devices tested. However, at least one manufacturer has

indicated that he is undertaking the development of a driving element capable of accepting microelectronic inputs and of performing level-changing and driving function for external data transmission.

CONCLUSIONS

1. Comparison of the output waveforms of the AN/UYK-1 to those of the integrated circuit logic elements showed that each of the microelectronic devices tested operated satisfactorily at the AN/UYK-1 frequency of 0.33 Mc/s. The Fairchild and General Instruments devices had better frequency response than the AN/UYK-1 circuits, but the Texas Instruments elements were somewhat slower.

2. The AN/UYK-1 operates at levels of zero to -13 volts while zero to +3 or +4 volt levels were common with the integrated circuits. While the implementation of the state counter function involved use of level-changing circuitry between AN/UYK-1 and microelectronic circuits, a computer designed to use integrated circuit elements exclusively in its logic and arithmetic sections would not require level-changing circuits except perhaps between logic and memory, or logic and input/output.

3. The supply voltage could be varied considerably without greatly affecting the operation of the integrated circuits. The Fairchild elements used to implement the state counter tolerated a V_{cc} power supply variation of 60 per cent. The Texas Instruments devices continued to operate satisfactorily with power supply variations of ±30 per cent. The General Instruments elements, which utilize three power supply voltages, withstood variations in V_{cc} of 31 per cent and in V_{cl} of 37 per cent, while variations in V_{bb} had practically no effect.

4. Means of packaging the integrated circuit elements were not investigated. In the course of breadboarding the Fairchild and General Instruments elements, leads were either soldered to terminal boards or inserted into subminiature sockets. The Texas Instruments devices were mounted on special holders with leads attached to the holder. These methods would not be satisfactory for high-density packaging of microelectronic devices and printed circuit boards or welded modules would be required under these conditions.

5. The only observations made on the cost of implementing AN/UYK-1 functions with integrated circuit elements were of component costs. Present prices are relatively high, but some reductions have been made and more are anticipated. Whether or not integrated circuit elements can compete with conventional circuitry depends upon the price of the elements, assembly costs, size of throw-away packages, and other factors.

6. Implementation of the logic functions of the AN/UYK-1 computer with some form of integrated circuit element is technically feasible. This conclusion is based on the facts that the elements performed satisfactorily at AN/UYK-1 frequencies, were not affected by noise, and were relatively insensitive to power supply variations. In addition, the elements have low power requirements and are capable of being densely packaged.

Navy Electronics Laboratory
Report 1144

MICROELECTRONIC LOGIC IMPLEMENTATION FOR THE AN/UYK-1 COMPUTER, by G. R. Potterf and W. G. Gannon. 41 p., 31 October 1962.

UNCLASSIFIED

Describes an investigation of the feasibility of constructing computer logic circuits with microelectronic integrated circuit elements. Certain portions of the AN UYK-1 computer were reproduced using off-the-shelf logic elements produced by Fairchild Semiconductor; Texas Instruments, Inc., and General Instruments Semiconductor. The experimental microelectronic circuits performed satisfactorily at the AN/UYK-1 operating frequencies, proved capable of withstanding considerable variations in power-supply voltage, and compared favorably with conventional circuits in power and space requirements. No attempt was made at this time to estimate the cost of using integrated circuit devices.

1. Model AN UYK-1
2. Microelectronics - Circuits

I. Potterf, G. R.
II. Gannon, W. G.

BuWeps Task 48415 (NEL R2-2)

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RECOMMENDATIONS

1. Investigate memory accession requirements and the feasibility of using integrated circuit devices in memory accession circuits.

2. Conduct studies of the practicality of using integrated circuit elements in input/output buffer applications.

3. Perform further research to determine the extent of cross talk and noise problems involved in large-scale use of microelectronic devices.

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